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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/411,792	10/01/1999	David Alan Eward	99-TK-238	8808

7590 06/02/2005	**EXAMINER**
Lisa K. Jorgenson, Esquire	VO, TED T
STMicroelectronics, Inc.	

1310 Electronics Drive	ART UNIT	PAPER NUMBER
Carrolton, TX 75006-5039	2192	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/411,792	EWARD ET AL.
	Examiner	Art Unit
	Ted T. Vo	2192

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>08 April 2005</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-64* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   This action is in response to the claimed amendment filed on 04/08/2005 responsive to Office

Action dated on 01/26/05.

Claims 1-64 stand finally rejected under 35 U.S.C. 102(b) as being anticipated by Circello et al.

(US No. 5,737,516).

Claims 1-64 are pending in the application.

Response to Arguments

2.   Applicants' arguments in the Remarks filed on 04/08/2005 have been fully considered.

Applicants alleged that Circello does not disclose "*a communication link coupling the processor

and debug circuit, wherein the processor is configured to transmit to the debug through the

communication link a plurality of bit values each representing a state of an operation in the processor

including at least an operand address*". Especially, Applicants argue Circello does not disclose "**an

operand address**".

Examiner would respectfully responds: It should be noted that the independent Claims 1, 21, 22,

42 (Remarks: page 4, Claim 1, page 5, Claims 21-22, page 6, Claim 42) comprise the feature above and

Applicants' argument is only relied on the claimed language "**operand address**" in the claimed limitation

"*bit values each representing a state of an operation in the processor including at least an operand

address*" for arguing the distinction. As seen in the scope of the Claims 1, 21, 22, 42, the claim

language, "**operand address**" is **mere data/information** in a trace buffer. This is only the binary bits

stored in the trace buffer called traced information. Within the scope of each independent Claims 1, 21,

22, or 42, this "**operand address**" (mere data) does nothing. In the applications' specification, **operand

address** appears also to be mere data and trace information (See spec: page 3, lines 4-6). In fact, the

trace buffer of the application's specification includes trace data such "operand address" and "instruction

address" (spec: page 4, lines 6-7).

It should be noted that,

In MPEP 2112.01, relating to content, matter, information which does nothing, the MPEP
indicates that "Where the only difference between a prior art product and a claimed product is
printed matter that is not functionally related to the product, the content of the printed matter will
not distinguish the claimed product from the prior art. In re Ngai, ___ F.3d ___, 2004 WL 1068957
(Fed. Cir. May 13, 2004)(Claim at issue was a kit requiring instructions and a buffer agent.
The Federal Circuit held that the claim was anticipated by a prior art reference that taught a kit
that included instructions and a buffer agent, even though the content of the instructions
differed.). See also In re Gulack, 703 F.2d 1381, 1385-86, 217 USPQ 401, 404 (Fed. Cir.
1983)("Where the printed matter is not functionally related to the substrate, the printed matter will
not distinguish the invention from the prior art in terms of patentability .... [T]he critical question is
whether there exists any new and unobvious functional relationship between the printed matter
and the substrate."

It is also noted that the recitation "operand address" in the Claims is only an intended use and

operand address does no structure different in compared to whatever data stored in the trace buffer of

Circello.

A recitation of the intended use of the claimed invention must result in a structural difference
between the **claimed** invention and the prior art in order to patentably distinguish the claimed
invention from the prior art. If the prior art structure is capable of performing the intended use,
then it meets the claim. In a claim drawn to a process of making, the intended use must result in
a manipulative difference as compared to the prior art. See In re Casey, 370 F.2d 576, 152
USPQ 235 (CCPA 1967) and In re Otto, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963).

Therefore, the "operand address" does not make distinguishable to any contents stored in the

trace buffer of the prior art Circello.

As cited by Examiner,

Claimed language "a communication link coupling the processor and debug circuit": Figure 2, all

connections/bus between core 9 and the debug module 10.

Claimed language "wherein the processor is configured to transmit to the debug through the

communication link a plurality of bit values each representing a state of an operation": Column 3, lines 54-

59, having means for transmit, operand address, representing a state.

Claimed language "in the processor including at least an operand address that indicates a memory

location at which an operand value is stored": Column 20, lines 27-61, particularly, take branch, value on

the CPST. Particularly, see: *capture an* <u>*instruction address*</u> *Target at the conclusion of the IC cycle of an instruction fetch pipeline* (at line 50-51).

See further: Col. 14, lines 65-67 and Col. 15, lines 1-23, real <u>trace function</u> that allows external user in developing/observing **"internal operations of data processor"** ect., DDATA signal provides data which reflects <u>operand data</u> , etc., DDATA signal provide provides capture instruction address program flow change, etc. It should be noted that this is the trace function that is associated with the trace data stored in the Circello's trace buffer. The teaching discloses more than **"operand address"** as claiming.

With regards to the Applicants argument,

"Applicants respectfully disagree that an operand address can be interpreted as an Instruction address. During the telephone interview, Applicants pointed out that although Circello may disclose sending instruction addresses from the core 9 to the debug circuit 10 (e.g., via the KADDR signal), an instruction address is very different from an operand address. An <u>instruction address specifies the memory location of an instruction</u>, while <u>an operand address specifies the memory location of an operand</u> on which the instruction operates. <u>These two addresses are different memory locations</u>. The operand value is stored at a different memory location from the instruction. Thus, the operand address is different from the instruction address."

Examiner respectfully disagrees: First of all "operand <u>address</u>", or "instruction <u>address</u>" is only the binary data/value obtained from a program counter. In Circello's column 22, within the table in line 27-35, it shows very clear the meaning of "instruction address" (right). It is a value of program counter. Each value points to a location of an "instruction". Each instruction may include an operator (such as Add, Mul, or Mov) and its operands. The Applicants' argument that "<u>These two addresses are different memory locations</u>" is incorrect.

As noted that the rejections of 21, 22, 42, particularly the recited limitation above, by referring the rejection of Claim 1 are proper because the Claims have the functionality corresponding to the functionality of Claim 1. Therefore all Applicants arguments to Claims 21, 22, and 42, are referred to the rationales above.

Applicants' arguments are not persuasive. Claims 1-64 stand finally rejected under 35 U.S.C. 102(b) as being anticipated by Circello et al. (US No. 5,737,516).

Claim Rejections - 35 USC § 102

3.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for

the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4.   Claims 1-64 are rejected under 35 U.S.C. 102(b) as being anticipated by Circello et al. (US No.

5,737,516), submitted by applicants.

Given the broadest reasonable interpretation of followed claims in light of the specification.

As per Claim 1:

Circello teaches, "*At least one processor* (FIG. 1, figure feature core 9);

a debug circuit (FIG. 1, all circuitries connecting to figure feature core 9);

a system bus coupling the processor and debug circuit (*See* FIG. 1, S-BUS, M-BUS, or K-BUS

etc. (*system bus*); and K-BUS, CPST, BUS REQUEST, BUS GRANT, STALL, BREAKPOINT CONTROL

(*communication link*)); *and*

a communication link coupling the processor and debug circuit (see figure 2, all connections/bus

between core 9 and the debug module 10), *wherein the processor is configured to transmit to the debug*

through the communication link a plurality of bit values each representing a state of an operation (see

Column 3, lines 54-59, having means for *transmit, operand address, representing a state*) *in the*

processor including at least an operand address that indicates a memory location at which an operand

value is stored (See column 20, lines 27-61, particularly, *take branch* , value on the CPST, *capture an*

instruction address Target at the conclusion of the IC cycle of an instruction fetch pipeline (operand

address; See Col. 14, lines 65-67 and Col. 15, lines 1-23).

As per Claim 2: Circello shows KCONTROLL and K-BUS that relates together in debugging, (column 4, lines 55-67), and discusses a pipeline operation that produces outputs to KADDR and KDATA of K-BUS (see column 6, lines 5-25).

As per Claim 3: In coupled with K-BUS, Circello discusses a register that stores program counter breakpoint (see column 9, lines 49-61).

As per Claim 4: Being inherent from debug mode operation (column 12, lines 35-39). Circello teaches that the counter program breakpoint defines a region in a local address space (see column 13, lines 37-50) belonged to a data processing system (FIG. 1) might be used to trigger breakpoint function. It further provides pipelines accessibility to cause a step instruction execution (see started column 19, line 64 to column 20, line 61).

As per Claim 5: Circello teaches inherently the limitation in discussing the trigger response (see column 29, lines 24-40).

As per Claim 6: Regarding limitation, "a first instruction past a branch instruction", Circello teaches inherently the limitation in using the value, %0101 of the PST signal (see column 15, lines 46-50).

As per Claim 7: Circello teaches inherently the limitation in using the values of the PST signal (see column 15, lines 46-50) for indicating branch or return instructions, where the PST receives information from K-BUS.

As per Claim 8: Circello discloses real-time tracing that provides a unique trace function (see column 22, lines 14-16).

As per Claim 9: Circello discloses a PST that receives information from K-BUS to provide bit information to reflect an execution status of the CPU (see column 15, lines 10-2).

As per Claim 10: Circello discloses the PST that receives information from K-BUS to assert some of bit values for exception processing (see FIG. 10).

As per Claim 11: Circello discloses the mechanism in the figure 2 that is configured to transmit debug information to the debug module via K-Bus and control links connected to the core 9.

As per Claim 12: Circello discloses the PST that receives information from K-BUS to assert bit values (FIG. 10). Some of these bit values indicate executions of instructions.

As per Claim 13: Circello discloses the PST that receives information from K-BUS to assert bit values

(FIG. 10). Some of these bit values indicate identifier information of executions. For example, one of bit

values indicates that a branch is taken.

As per Claim 14: Circello provides debugging which is capable of performing exception/interrupt handling

(FIG. 10, or column, 8, lines 35-41).

As per Claim 15: Claims limitation is inherent in bits values. For example, the signal from K_BUS causes

the control 60 to generate PST and DDATA. The table in columns 22-23 describes bit values of the

DDATA, where these values are used by external development system to view the execution of

instructions.

As per Claim 16: For a matching with a memory address access by the processor in response to an

execution instruction is inherent in branching/jumping or exception/interrupt.

As per Claim 17: Being inherent in execution of single instruction step mode (column 11, lines 55-56) or

the status that indicates, 'begin execution of an instruction' (FIG. 10).

As per Claim 18: Circello discloses the PST that receives information from K-BUS to assert bit values

(FIG. 10). Some of these bit values indicate identifier information of executions. For example, one of bit

values indicates that a branch is taken.

As per Claim 19: Being inherent in execution of tracing function (see column 22, lines 14-25) or the status

that indicates, 'begin execution of an instruction' (FIG. 10).

As per Claim 20: FIG. 1 has means of a single integrated circuit.

As per Claim 21:

Circello discloses, "At least one processor (FIG. 1, figure feature core 9);

            a debug circuit (FIG. 1, all circuitries connecting to figure feature core 9);

            a system bus coupling the processor and debug circuit (See FIG. 1, S-BUS, M-BUS, or K-BUS

etc (system bus)); and

            a communication link coupling the processor and debug circuit (See FIG. 1, K-BUS, CPST, BUS

REQUEST, BUS GRANT, STALL, BREAKPOINT CONTROL (communication link), where the processor

is configured to transmit to the debug through the communication link a plurality of bit values each

representing a state of an operation in the processor including at least one of: and

an operand address that indicates a memory location at which an operand value is stored (See

Col. 14, lines 65-67 and Col. 15, lines 1-23); *and an operand value* (*See* column 20, lines 27-61,

particularly, *take branch*, value on the CPST, "capture an <u>instruction address Target</u> at the conclusion of

the IC cycle of an instruction fetch pipeline": '*operand address and operand value*');

where the processor is further to configured to transmit to the debug circuit: a program counter

value indicating the program counter of the processor at a writeback stage of a pipeline of the processor,

a status indicating that a computer instruction is in the writeback stage is valid computer instruction (*See,*

Column 20, lines 27-62, *pipeline, instruction address of "Target". As the JMP instruction occupies the*

AGEX stage of the operand execution pipelines; see column 13, lines 37-64, Program Counter

Breakpoint, data signal transferred via K-Bus 25..."); *a status indicating that the computer instruction in*

the writeback stage is a first instruction past an execute branch instruction; a status indicating a type of

executed branch instruction and process identifier information of an executed instruction (*See* started

from column 12, line 15 to column 13, line 64, teaching of address space that defines a range started with

a breakpoint location; and see DDATA bit definitions, the table in columns 22-23).

<u>As per Claims 22, 42</u>: The claims have the claimed functionality corresponding to the functionality of

Claim 1. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 1.

<u>As per Claims 23, 43</u>: The claims have the claimed functionality corresponding to the functionality of

Claim 2. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 2.

<u>As per Claim 24</u>: The claim has the claimed functionality corresponding to the functionality of Claim 3.

Claim is rejected in the same reasons set forth in connecting to the rejection of Claim 3.

<u>As per Claims 25, 44</u>: The claims have the claimed functionality corresponding to the functionality of

Claim 4. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 4.

<u>As per Claims 26, 45</u>: The claims have the claimed functionality corresponding to the functionality of

Claim 5. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 5.

<u>As per Claims 27, 46</u>: The claims have the claimed functionality corresponding to the functionality of

Claim 6. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 6.

<u>As per Claim 28, 47</u>: The claims have the claimed functionality corresponding to the functionality of Claim

7. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 7.

<u>As per Claim 29, 48</u>: The claims have the claimed functionality corresponding to the functionality of Claim

8. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 8.

<u>As per Claims 30, 49</u>: The claims have the claimed functionality corresponding to the functionality of

Claim 9. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 9.

<u>As per Claims 31, 50</u>: The claims have the claimed functionality corresponding to the functionality of

Claim 10. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 10.

<u>As per Claims 32, 51</u>: The claims have the claimed functionality corresponding to the functionality of

Claim 11. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 11.

<u>As per Claims 33, 52</u>: The claims have the claimed functionality corresponding to the functionality of

Claim 12. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 12.

<u>As per Claims 34, 53</u>: The claims have the claimed functionality corresponding to the functionality of

Claim 13. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 13.

<u>As per Claims 35, 54</u>: The claims have the claimed functionality corresponding to the functionality of

Claim 14. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 14.

<u>As per Claims 36, 55</u>: The claims have the claimed functionality corresponding to the functionality of

Claim 15. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 15.

<u>As per Claims 37, 56</u>: The claims have the claimed functionality corresponding to the functionality of

Claim 16. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 16.

<u>As per Claims 38, 57</u>: The claims have the claimed functionality corresponding to the functionality of

Claim 17. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 17.

<u>As per Claims 39, 58</u>: The claims have the claimed functionality corresponding to the functionality of

Claim 18. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 18.

As per Claims 40, 59: The claims have the claimed functionality corresponding to the functionality of Claim 19. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 19.

As per Claims 41, 60: The claims have the claimed functionality corresponding to the functionality of Claim 20. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 20.

As per Claim 61: Circello discloses the claim limitation (See column 20, lines 27-61, particularly, *take branch*, value on the CPST, *capture an instruction address Target at the conclusion of the IC cycle of an instruction fetch pipeline* (operand address and operand value); and see FIG.2, the K-BUS connected to the to the FIFO 70; and see Col. 14, lines 65-67 and Col. 15, lines 1-23).

As per Claim 62: Circello discloses the claim limitation (See column 20, lines 27-61, particularly, *take branch*, value on the CPST, *capture an instruction address Target at the conclusion of the IC cycle of an instruction fetch pipeline* (operand address and operand value); and see FIG.2, the K-BUS connected to the to the FIFO 70, and see Col. 14, lines 65-67 and Col. 15, lines 1-23);

As per Claims 63, 64: The claims have the claimed functionality corresponding to the functionality of Claim 62. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 62.

Conclusion

5.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

        A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (571) 272-3706. The examiner can normally be reached on 8:00AM to 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3694. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted T. Vo
Primary Examiner
Art Unit 2192
May 31, 2005